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PATENT, TRADEMARK
AND COPYRIGHT LAW

FACSIMILE: (703) 684-1157

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(703) 684-1120

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24956

PATENT TRADEMARK OFFICE

To: Assistant Commissioner for Patents
Washington, D.C. 20231

Sir: Transmitted herewith for filing is the patent application of:

Inventor: T. SASAKI et al (See Attached List)

For:
DESIGN METHOD AND SYSTEM FOR SEMICONDUCTOR INTEGRATED CIRCUITS

Enclosed are:



7 Sheets of Drawings



This application is being filed without an executed Declaration.



Priority is claimed from Japanese Application No. 2001-038678
filed February 15, 2001. A certified copy is attached herewith.



Copies of the disclosure documents listed on the attached PTO 1449 form and
 discussed in the specification or attached Information Disclosure Statement.



A verified statement to establish small entity status under 37 CFR 1.9 and 1.27.



Specification: Abstract , Description 22 pages; and 15 claim(s).



Preliminary Amendment.



Executed Declaration.

The filing fee is calculated as shown below:

Small Entity

Large Entity

For:	No. Filed	No. Extra
Basic Fee		
Total Claims	15 -20 =	* 0
Indep Claims	5 - 3 =	* 2
<input type="checkbox"/> Multiple Dependent Claim (s)		

Rate	Fee
	\$ 370
x 9	\$
x 42	\$
+ 140	\$
Total	\$

OR

Rate	Fee
	\$ 740
x 18	\$ 0
x 84	\$ 168
+ 280	\$ 0
Total	\$ 908

* If difference is less than zero
then enter '0' in second column



A check in the amount of \$ 908.00 is enclosed for the filing fee.



The Commissioner is hereby authorized to charge any additional fees that may be required to
Deposit Account No. 50-1417.

Respectfully Submitted,

By:

John R. Mattingly
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LIST OF INVENTORS' NAMES AND ADDRESSES

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